wherein an impurity concentration of the channel region is equal to or less than an impurity concentration in the drift region, and a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region.

REMARKS

Claims 1, 4, 12 and 20-30 are pending. By this Amendment, claims 2 and 3 are canceled; claims 1, 4 and 12 are amended; and new claims 20-30 are added. Reconsideration and allowance are respectfully requested in view of the above amendments and the following remarks.

The attached Appendix includes a marked-up copy of each amended claim (37 C.F.R. 1.121(c)(ii)).

Allowable Subject Matter

Applicant gratefully acknowledges that the Office Action indicates that claim 12 is allowed. Claim 12 is amended to recite "a source region having the second conductive type" (emphasis added). Instant claim 12 is believed to be allowable.

For the reasons stated below, Applicant respectfully submits that all pending claims are allowable.

Rejection Under 35 U.S.C. § 102

The Office Action rejects claims 1 and 3 under 35 U.S.C. § 102(b) over Terashima. Claim 3 is canceled. Claim 1 is amended to include the features of claim 2. Accordingly, this rejection is moot.

Rejection Under 35 U.S.C. § 103

The Office Action rejects claims 2 and 4 under 35 U.S.C. § 103(a) over Terashima. Applicant respectfully traverses this rejection.

As stated above, instant claim 1 includes the features of canceled claim 2. Claim 4 depends from claim 1. Terashima fails to teach or suggest the semiconductor device of claim 1 for the following reasons.

Instant claim 1 recites "the gate region formed of a p+-type semiconductor". As shown, for example, in Fig. 14 of Terashima, the semiconductor device includes a control electrode 6. Terashima does not disclose or suggest that the control electrode 6 is a semiconductor. Terashima also does not disclose or suggest a gate region that is formed of a p+-type semiconductor. The built-in potential between a gate that is a p+-type semiconductor and a channel region is higher than that of a gate with n+-type semiconductor and a channel region. Consequently, the p+ gate enables turn off even if an interval of the p+ gate is wide.

For the above reasons, claim 1 is believed to be allowable over Terashima. Claim 4 depends from claim 1 and thus is also allowable. Therefore, Applicant respectfully requests that this rejection be withdrawn.

New Claims

New claims 20-30 are also allowable. Independent claim 20 includes combined features of claims 1 and 5. As discussed at page 7, lines 12-20 of the present specification, the embodiment of claim 20 makes it possible to omit a forming process of the p+-type source region. See also Fig. 7.

Independent claim 21 includes combined features of claims 1 and 7. As discussed at page 7, line 29 to page 8, line 2 of the specification, the embodiment of claim 21 enables changing the resistance of the n+-type extension region material. Accordingly, an appropriate

source resistance is formed, which allows automatic adjustment of current balance between the transistors. See also Fig. 8. Accordingly, claim 21 is believed to also be allowable.

Claims 22-29 depend directly or ultimately from claim 12, and recite the features of claims 2 and 4-10, respectively. Accordingly, claims 22-29 are allowable for at least the same reasons as stated above for claim 12.

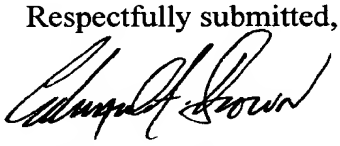
Support for the features recited in original claims 5-7, which are now incorporated in the above-described new claims, can be found in Figs. 5, 7c and 8.

Independent claim 30 is similar to instant claim 12. However, claim 30 recites "a channel region having a first conductive type" (emphasis added).

For the foregoing reasons, Applicant respectfully requests reconsideration and withdrawal of the rejections and prompt allowance of the pending claims.

Should the Examiner believe that anything further is desirable to place the application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the number listed below.

Respectfully submitted,



James A. Oliff
Registration No. 27,075

Edward A. Brown
Registration No. 35,033

JAO:EAB/ldg

Attachment:
Appendix

Date: November 8, 2001

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

APPENDIX

Changes to Claims:

Claims 2 and 3 are canceled.

Claims 20-30 are added.

The following are marked-up versions of the amended claims:

1. (Twice Amended) A bipolar semiconductor device comprising:

a drain electrode;

a drain region ~~having a first conductive type~~ formed of a p+-type semiconductor and disposed on the drain electrode;

a drift region having a second conductive type different from the ~~first~~ conductive type of the drain region and disposed on the drain region;

a channel region having the second conductive type and disposed on the drift region;

a gate region ~~provided so as to surround~~ surrounding at least a part of the channel region via an insulation film, the gate region formed of a p+-type semiconductor;

a source region having the second conductive type provided on the channel region, the source region is located substantially at a center of the channel region, and the source region is isolated from the insulation film; and

a source electrode connected to the source region,

wherein a depletion layer is formed over most of the entire channel region when a predetermined voltage is applied to the gate region.

4. (Amended) The semiconductor device according to claim ~~2~~ 1, further comprising a semiconductor region ~~having the first conductive type~~ formed of a p+-type semiconductor and provided between the channel region and the source region.

12. (Three Times Amended) A semiconductor device comprising:

a substrate having a first conductive type;

a drift region having the first conductive type and disposed on the substrate;

a channel region having a second conductive type different from the first conductive type and provided on the drift region;

a gate region provided so as to surround at least the channel region via an insulation film; and

a source region having the ~~first~~ second conductive type and provided on the channel region, the source region is located substantially at a center of the channel region, and ~~wherein~~ the source region is isolated from the insulation film, wherein:

an impurity concentration of the channel region is equal to or less than an impurity concentration in the drift region, and a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region.